

AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior listings, and all prior versions, of claims in the application.

Listing of Claims:

1. – 21. (Canceled)

22. (Previously Presented) A fabrication method of a semiconductor integrated circuit device, comprising the steps of:

(a) depositing a silicon oxide insulating film over a patterned silicon nitride film with a doped polycrystalline silicon plug over a semiconductor substrate;

(b) forming a hard mask over said silicon oxide insulating film; and

(c) subjecting said semiconductor substrate to a plasma etching treatment through the hard mask as an etching mask using an etching gas containing a fluorocarbon gas, oxygen and a dilution gas to process said silicon oxide insulating film, so as to form a hole in said silicon oxide insulating film down to the patterned silicon nitride film in such a manner that an upper surface of the doped polycrystalline silicon plug is exposed,

wherein a residence time of the etching gas within an etching chamber is set at 50 to 700 ms.

23. (Original) A method according to Claim 22, wherein a pressure within the chamber during the plasma etching ranges from 0.7 to 7 Pa.

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24. (Original) A method according to Claim 22, wherein a total flow rate of the etching gas passed into the etching chamber ranges from 200 to 1000 cm³/minute.

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25. (Original) A method according to Claim 22, wherein a total flow rate of the etching gas passed into the etching chamber is at 700 cm³/minute or over.

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26. (Original) A method according to Claim 22, wherein a pressure within the etching chamber during the plasma etching ranges from 1.3 to 4 Pa, and the total flow rate of the etching gas passing into the etching chamber is at 700 cm³/minute or over.

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27. (Original) A method according to Claim 22, wherein a flow rate of said dilution gas is larger than the flow rates of said fluorocarbon gas and oxygen.

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28. (Original) A method according to Claim 22, wherein a plasma density during the plasma etching ranges from 1×10^{10} to $1 \times 10^{13}/\text{cm}^3$.

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29. (Original) A method according to Claim 22, wherein a plasma density during the plasma etching ranges from 1×10^{10} to $1 \times 10^{12}/\text{cm}^3$.

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30. (Original) A method according to Claim 22, wherein said fluorocarbon gas is made of C₅F₈, and said dilution gas is made of argon.

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31. (Original) A method according to Claim 30, wherein a flow rate of said argon gas ranges from 200 to 1000 cm³/minute.

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32. (Original) A method according to Claim 30, wherein a flow rate of said argon gas ranges from 400 to 800 cm³/minute.

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33. (Original) A method according to Claim 30, wherein a ratio in flow rate between the oxygen and C₅F₈ (oxygen/C₅F₈) ranges from 0.8 to 1.5.

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34. (Original) A method according to Claim 30, wherein a ratio in flow rate between the oxygen and C₅F₈ (oxygen/C₅F₈) ranges from 1 to 1.2.

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35. (Original) A method according to Claim 30, wherein a partial pressure of C₅F₈ ranges from 0.02 to 0.2 Pa.

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36. (Original) A method according to Claim 30, wherein a partial pressure of C₅F₈ ranges from 0.04 to 0.1 Pa.

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37. (Previously Presented) A fabrication method of a semiconductor integrated circuit device, comprising the steps of:

- (a) depositing a silicon oxide insulating film over a patterned silicon nitride film with a doped polycrystalline silicon plug over a semiconductor substrate;
- (b) forming a hard mask over said silicon oxide film; and

(c) subjecting the semiconductor substrate to a plasma etching treatment through the hard mask as an etching mask using an etching gas containing a fluorocarbon gas, oxygen and a dilution gas to process said silicon oxide insulating film, so as to form a hole in said silicon oxide insulating film down to the patterned silicon nitride film in such a manner that an upper surface of the doped polycrystalline silicon plug is exposed,

wherein a residence time of the etching gas within an etching chamber is set at 50 to 350 ms.

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38. (Previously Presented) A fabrication method of a semiconductor integrated circuit device, comprising the steps of:

(a) depositing a silicon oxide insulating film over a patterned silicon nitride film with a doped polycrystalline silicon plug over a semiconductor substrate;

(b) forming a hard mask over said silicon oxide film; and

(c) subjecting the semiconductor substrate to a plasma etching treatment through the hard mask as an etching mask using an etching gas containing a fluorocarbon gas, oxygen and a dilution gas to process said silicon oxide insulating film, so as to form a hole in said silicon oxide insulating film down to the patterned silicon nitride film in such a manner that an upper surface of the doped polycrystalline silicon plug is exposed,

wherein a residence time of the etching gas within an etching chamber is set at 100 to 200 ms.

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39. (Previously Presented) A fabrication method of a semiconductor integrated circuit device, comprising the steps of:

- (a) depositing a silicon oxide insulating film over a patterned silicon nitride film with a doped polycrystalline silicon plug over a semiconductor substrate;
- (b) forming a hard mask over said silicon oxide film; and
- (c) subjecting the semiconductor substrate to a plasma etching treatment through the hard mask as an etching mask using an etching gas containing a fluorocarbon gas, oxygen and a dilution gas to process said silicon oxide insulating film, so as to form a hole in said silicon oxide insulating film down to the patterned silicon nitride film in such a manner that an upper surface of the doped polycrystalline silicon plug is exposed,

wherein a pressure within the etching chamber during the plasma etching ranges from 0.7 to 7 Pa and a total flow rate of the etching gas passed into the etching chamber is 700 cm³/minute or over.

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40. (Previously Presented) A fabrication method of a semiconductor integrated circuit device, comprising the steps of:

- (a) depositing a silicon oxide insulating film over a patterned silicon nitride film with a doped polycrystalline silicon plug over a semiconductor substrate;
- (b) forming a hard mask over said silicon oxide film; and
- (c) subjecting the semiconductor substrate to a plasma etching treatment through the hard mask as an etching mask using an etching gas containing a fluorocarbon gas, oxygen and a dilution gas to process said silicon oxide insulating film, so as to form a hole in said silicon oxide insulating film down to the patterned

silicon nitride film in such a manner that an upper surface of the doped polycrystalline silicon plug is exposed,

wherein a pressure within the etching chamber during the plasma etching ranges from 1.3 to 4 Pa and a total flow rate of the etching gas passed into the etching chamber is 700 cm³/minute or over.